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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
VINH, LAN

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 10/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,439	COOLBAUGH ET AL.	
	Examiner	Art Unit	
	Lan Vinh	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-7, 9, 11-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Eklund et al (US 5,656,524)

Eklund discloses a method for forming a polysilicon resistor. The method comprises the steps of:

providing a structure that includes at least one polysilicon resistor device region 20 and at least one other type of device region, said at least one polysilicon resistor device region comprising a polysilicon layer (col 3, lines 44-46; col 5, lines 1-5)

selectively performing an ion implant and activation anneal in the at least one other type of device region (col 4, lines 38-48), forming one emitter of a bipolar transistor (col 4, lines 32-36)

forming a protective dielectric layer 24 overlying the polysilicon layer in the polysilicon resistor device region (col 5, lines 3-6; fig. 3a)

providing a predetermined resistance value to the polysilicon layer in the one polysilicon resistor device region (col 2, lines 20-22)

Regarding claim 2, Eklund discloses one polysilicon device region comprises a semiconductor substrate, the polysilicon layer located on the substrate and a dielectric layer 22 located on the polysilicon layer (col 5, lines 4-5)

Regarding claim 3, Eklund discloses wherein the other device region comprise a CMOS devices (col 3, lines 53-54)

Regarding claim 4, Eklund discloses forming a patterned photoresist 26 atop the at least one polysilicon resistor device region to protect the region during said selective ion implant (fig. 6)

Regarding claim 5, Eklund discloses the protective dielectric layer is a nitride (col 5, lines 5-6)

Regarding claim 6, Eklund discloses the step of providing resistance value to said polysilicon layer comprises ion implantation into the polysilicon layer (col 4, lines 37-38)

Regarding claim 7, Eklund discloses implanting with n-type dopant (col 5, lines 40-43)

Regarding claim 9, Eklund discloses performing an annealing step after said ion implantation (col 4, lines 45-48)

Regarding claim 11, Eklund discloses exposing end portions of the polysilicon layer (col 7, lines 17-18)

Regarding claims 12-13, Eklund discloses performing a silicidation process to form silicide contact on the exposed polysilicon (col 5, lines 28-30)

Regarding claim 14-16, Eklund discloses forming a conductive layer of Ti and performing an anneal to cause reaction of the Ti with the polysilicon layer to form silicide (col 6, lines 10-20)

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eklund et al (US 5,656, 524) in view of Gardner et al (US 6,027, 964)

Eklund method has been described above. Unlike the instant claimed invention as per claim 8, Eklund fails to specifically disclose that the ion implantation provides the polysilicon layer with a dopant concentration of from about $1x10^{14}$ to about $1x10^{21}$ atom/cm3.

Gardner discloses a method for making an FET comprises the step of the ion implanting the polysilicon layer with a dopant concentration of from about $1x10^{15}$ atom/cm3 (col 6, lines 40-41)

Hence, one skilled in the art at the time the invention was made would have found it obvious to modify Eklund method by implanting the polysilicon layer with a dopant concentration as per Gardner because Gardner discloses that the polysilicon can be doped by implanting with a dosage in the range of $1x10^{15}$ to about $5x10^{15}$ atoms/cm3 (col 6, lines 38-40)

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eklund et al (US 5,656, 524) in view of Segawa et al (US 6,436,747)

Eklund method has been described above. Unlike the instant claimed invention as per claim 10, Eklund fails to specifically disclose that the annealing step is performed in an inert gas ambient that may optionally be mixed with less than about 10% oxygen

Segawa discloses a method for fabricating semiconductor device comprises the step of annealing the polysilicon in nitrogen/inert gas and oxygen (col 8, lines 39-44)

Thus, one skilled in the art at the time the invention was made would have found it obvious to modify Eklund method by annealing the polysilicon in nitrogen/inert gas and oxygen as per Segawa because according to Segawa, the out-diffusion of the n-type impurity is suppressed during the RTA process containing oxygen (col 11, lines 4-7)

6. Claim 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eklund et al (US 5,656, 524) in view of Segawa et al (US 6,436,747)

Eklund discloses a method for forming a polysilicon resistor. The method comprises the steps of:

providing a structure that includes at least one partially polysilicon resistor device region 20 and at least one other type of device region, said at least one polysilicon resistor de-vice region comprising a polysilicon layer (col 3, lines 44-46; col 5, lines 1-5), performing an annealing step on the wafer (col 4, lines 45-48), forming one emitter of a bipolar transistor (col 4, lines 32-36)

depositing a protective layer 24/ SiN over the polysilicon layer to protect the polysilicon layer against subsequent silicide processing (col 5, lines 3-6; fig. 3a)

ion implating a dopant into the poysilicon layer through the SiN/protective layer (col 6, lines60-65)

performing silicide processing to form the precision polysilicon resistor (col 5, lines 28-30)

Unlike the instant claimed invention as per claim 17, Eklund fails to specifically disclose performing a RTA for an emitter/FET activation process on a wafer/emitter of a bipolar transistor

Segawa discloses a method for fabricating semiconductor device comprises the step of performing a RTA on a FET device (col 6, lines 5-8)

Thus, one skilled in the art at the time the invention was made would have found it obvious to modify Eklund method by performing a RTA for an emitter process/ emitter of a bipolar transistor (col 4, lines 32-36) in view of Segawa teaching because according to Segawa, the out-diffusion of the n-type impurity is suppressed during the RTA process containing oxygen (col 11, lines 4-7)

The limitation of claim 17 has been discussed above

Regarding claims 18-19, Eklund discloses forming a conductive layer of Ti and performing an anneal to cause reaction of the Ti with the polysilicon layer to form silicide (col 6, lines 10-20)

Response to Arguments

7. Applicant's arguments filed 8/4/2005 have been fully considered but they are not persuasive.

Applicants argue that claim 1 is not anticipated by the disclosure of Eklund because Eklund discloses a different processing sequence then the methodology recited in amended claim 1 that requires the emitter is ion implanted and annealed prior to provide the predetermined resistance value to the polysilicon layer in the resistor device region. This argument is unpersuasive because it does not commensurate with the scope of claim 1 since claim 1 does not require/recite that the emitter is ion implanted and annealed prior to provide the predetermined resistance value to the polysilicon layer in the resistor device region. In addition, by lacking of a clear indication of a specific sequential required for the claimed steps, recited in claim 1, the claim language of "comprising" does not limit the claimed steps to be performed in any specific processing sequences. Thus, it is asserted that the steps, recited in Eklund method, anticipates amended claim 1

Applicants argue that claim 17 is not render obvious by Eklund and Segawa because Eklund does not disclose forming an activated emitter region prior to providing a predetermined resistance value into the polysilicon layer of the resistor device region and there is no motivation in the applied references which suggest modifying the disclosed methods to include the processing sequence recited in claim 17. This argument is unpersuasive because it does not commensurate with the scope of claim 17 since claim 17 language does not require/recite forming an activated emitter region prior to providing a predetermined resistance value into the polysilicon layer of the resistor device region or the claimed steps have to performed in a specific processing sequence.

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 571 272 1471. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571 272 1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LV
October 6, 2005